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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/528,524	03/20/2000	Jacques Michelet	B-3881-617765-1	5142

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Richard J Pacuilan
Ladas & Parry
5670 Wilshire Boulevard
21st Floor
Los Angeles, CA 90036

EXAMINER	
PHAM, THOMAS K	
ART UNIT	PAPER NUMBER
2121	12

DATE MAILED: 07/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/528,524	MICHELET ET AL.	
	Examiner	Art Unit	
	Thomas K Pham	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Notice to Applicant(s)

1. Claims 1-20 of U.S. Application 09/528524 filed on 20 March 2000 are presented for examination.

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

DETAILED ACTION

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 6 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim U.S. Patent No. 5,670,972.

5. As for claim 1, Kim discloses a communication process between an Information Handling System (IHS) and at least one display having On Screen Display (OSD) capability (abstract); wherein said IHS system includes a processor (fig. 1, element 7) under control of an operating system, a graphics system (col. 3 lines 22-27) and an electronic circuit operating independently of said processor arid said graphics system (col. 2 lines 44-59), said at least one display receives a graphics channel comprising the graphic signals generated by said graphics system and a service channel allowing interaction between said at least one display and said operating system (col. 3 lines 53-67); the process being characterized in that said service channel is also used to permit said independent electronic circuit to have access to the On Screen Display

(OSD) capability of said at least one display in order to display text and/or graphics independently of said processor and said operating system (col. 5 lines 18-29 and col. 3 lines 7-10).

6. As for claim 6, Kim discloses an information Handling System (IHS) comprising: a processor (fig. 1, element 7) arranged to operate under the control of an operating system, a graphics system (col. 3 lines 22-27) and an electronic circuit operable independently of said processor (col. 2 lines 44-59); at least one display having On Screen Display (OSD) capability and including first receiving means for receiving a graphics channel upon which graphics signals generated by said graphics system are transmitted, and second receiving means for receiving a service channel for allowing interaction between said at least one display and said operating system (col. 3 lines 53-67); characterized in that said service channel and said display are arranged to permit said independent electronic circuit to access the On Screen Display (OSD) capability of said at least one display in order to display text and/or graphics independently of said processor and said operating system (col. 5 lines 18-29 and col. 3 lines 7-10).

7. As for claim 15, Kim discloses a display device having On Screen Display (OSD) capability for use in an Information Handling System (IHS) including a processor (fig. 1, element 7) under control of an operating system, a graphics system (col. 3 lines 22-27) and an electronic circuit operating independently of said processor and said graphics system (col. 2 lines 44-59), said display having one or more connectors for receiving a graphics channel comprising graphics signals generated by said graphics system (col. 3 lines 28-30) and a service channel allowing interaction between said display and said operating system; characterized by means

responsive to commands in said service channel for controlling the On Screen Display capability independently of the operation of the processor and the operating system (col. 3 lines 31-37).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-3, 5, 7-9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of "VESA Display Data Channel Command Interface (DDC/CI) Standard" (hereinafter VESA).

10. As to claim 2, Kim does not specifically disclose the display consists of "*a bi-directional serial communication link which is compatible with the IC protocol, providing either DDC or DDC/CI communication support with said operating system*", as well as an I^2C communication link between said independent electronic circuit and said at least one display in order to provide to said electronic circuit and a direct access to the OSD capability of said at least one display. However, VESA teaches the use of DDC/CI offers bi-directional communication between the computer graphic host and the display device (see page 1, Summary) using I^2C communication. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the bi-directional communication DDC/CI of VESA into the independent electronic circuit of Kim in order to maximize reliability and system uptime by providing

information in a compact and scalable format to allow the graphic sub-system to be configured based on the capabilities of the attached display.

11. As for claim 3, Kim discloses a process according to claim 2 characterized in that said electronic circuit consists of a hardware monitoring circuit displaying monitoring feedback information to the user via said service channel (col. 5 lines 18-29).

12. As for claim 5, the process according to claim 3 characterized in that said hardware monitoring circuit is connected via a network to said IHS system in order to provide an alarm on Local Area Network (LAN) capability. Although the invention has been describes with a certain degree of particularity, it should be recognized that elements thereof may be altered by persons skilled in the art by applying the monitoring circuit into a local area network when desired by the user without departing from the spirit and scope of the invention.

13. As for claim 7, information Handling System according to claim 6 characterized in that said service channel consists of a bi-directional serial communication link, which VESA discloses the interaction between the display and its graphic host (see page 9, Summary).

14. As for claim 8, information handling system as claimed in claim 7 wherein said serial communication link is compatible with the I^2C protocol, and provides a DDC or a DDC/CI communication interface with said processor as well as an I^2C communication link between said independent electronic circuit and said at least one display in order to provide to said electronic circuit a direct access to the OSD capability of said at least one display, which VESA discloses DDC/CI display control interface level (see page 11).

15. As for claim 9, Kim discloses an information handling system according to claim 7 characterized in that said electronic circuit is a hardware monitoring circuit for displaying monitoring feedback information to the user via said service channel (col. 5 lines 18-29).

16. As to claim 16, Kim does not specifically disclose the display consists of "*a bi-directional serial communication link which is compatible with the IC protocol, providing either DDC or DDC/CI communication support with said operating system*", as well as an I^2C communication link between said independent electronic circuit and said at least one display in order to provide to said electronic circuit and a direct access to the OSD capability of said at least one display. However, VESA teaches the use of DDC/CI offers bi-directional communication between the computer graphic host and the display device (see page 1, Summary) using I^2C communication. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the bi-directional communication DDC/CI of VESA into the independent electronic circuit of Kim in order to maximize reliability and system uptime by providing information in a compact and scalable format to allow the graphic sub-system to be configured based on the capabilities of the attached display.

17. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of "HP MaxiLife: for the Highest Productivity and Reliability" (hereinafter HP-MaxiLife) and in further view of Nelson U.S. Patent No. 5,768,612.

18. As for claim 4, Kim does not specifically disclose a process according to claim 1 characterized in that said graphics system is either an AGP or PCI graphics card which is plugged into a corresponding AGP or PCI slot having at least two conductors being reserved for said I^2C communication link conveying the OSD commands to be directed to said at least one

display. However, HP-MaxiLife discloses the I^2C communication link (figure of page 4). Further more, Nelson discloses a graphic accelerator is a PCI graphics card which is plugged into a corresponding PCI slot having at least two conductors (col. 4 lines 14-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the I^2C communication link of HP-MaxiLife with the On Screen Display (OSD) of Kim in order to make it simple and easy to gather information about a computer's components. In addition, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PCI buses of Nelson with the I^2C communication link of HP-MaxiLife and the On Screen Display (OSD) of Kim in order to utilized the high bandwidth and flexibility that is independent of new processor technologies and increases processor speed.

19. Claim 10, 13-14 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of VESA and in further view of Fisch et al. U.S. Patent No. 5,901,297 (hereinafter Fisch).

20. As to claim 10, the Information Handling System (IHS) comprising all the limitations as discussed above in claim 8 characterized in that said graphics systems except that the combination of Kim and VESA fails to disclose an arbitration means having a first input connected to receive said first I^2C communication channel provided by said graphics engine, and having a second input for receiving a second I^2C communication channel provided by said hardware monitoring circuit; said arbitration means providing arbitration between said first and said second I^2C communication links so that the hardware monitoring circuit and the processor can both get access to said second receiving means of said at least one display. However, Fisch teaches the use of an initialization mechanism for symmetric arbitration agents (see arbitration

unit 320 in Fig. 3). The arbitration counter of each bus agent is used to keep track of which agent was the last or current owner of the bus and which agent will be the next owner of the bus (col. 2, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the arbitration means of Fisch into the computer system of Kim and VESA in order to improve the efficiency of the hardware monitoring systems by systematically assigning a priority level to each of the multiple agents on a bus.

21. As to claim 13, Kim discloses the Information Handling System (IHS) as recited in claim 6 characterized by: a graphics engine for providing graphics signals to said graphics channel (col. 3 lines 22-27) for controlling said at least one display. Kim does not specifically disclose a first I^2C communication channel complying with the DDC/CI protocol; an arbitration means having a first input connected to receive said first I^2C communication channel provided by said graphics engine, and having a second input for receiving a second I^2C communication channel provided by said hardware monitoring circuit; said arbitration means providing arbitration between said first and said second I^2C communication links so that the hardware monitoring circuit and the processor can both get access to said second receiving means of said at least one display. However, VESA discloses a first I^2C communication channel complying with the DDC/CI protocol (page 1, Summary). Furthermore, Fisch teaches the use of an initialization mechanism for symmetric arbitration agents (see arbitration unit 320 in Fig. 3). The arbitration counter of each bus agent is used to keep track of which agent was the last or current owner of the bus and which agent will be the next owner of the bus (col. 2, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the first I^2C communication DDC/CI protocol of VESA into the independent electronic circuit of

Kim in order to maximize reliability and system uptime by providing information in a compact and scalable format to allow the graphic sub-system to be configured based on the capabilities of the attached display. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the arbitration means of Fisch into the computer system of Kim and VESA in order to improve the efficiency of the hardware monitoring systems by systematically assigning a priority level to each of the multiple agents on a bus.

22. As for claim 14, a graphics system according to claim 13 characterized in that said arbitration means are arranged to prevent the access of said service channel to one among said first and second I^2C communication links until a preceding I^2C transaction has been successfully completed. This process is interpreted as an operable connection is achieved and memory status: obtained by system component such as a device arbiter, tracking past memory access activities and inferring the status of one or more memory devices from that past activity.

23. As to claim 17, the Information Handling System (IHS) comprising all the limitations as discussed above in claim 7 characterized in that said graphics systems except that the combination of Kim and VESA fails to disclose an arbitration means having a first input connected to receive said first I^2C communication channel provided by said graphics engine, and having a second input for receiving a second I^2C communication channel provided by said hardware monitoring circuit; said arbitration means providing arbitration between said first and said second I^2C communication links so that the hardware monitoring circuit and the processor can both get access to said second receiving means of said at least one display. However, Fisch teaches the use of an initialization mechanism for symmetric arbitration agents (see arbitration

unit 320 in Fig. 3). The arbitration counter of each bus agent is used to keep track of which agent was the last or current owner of the bus and which agent will be the next owner of the bus (col. 2, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the arbitration means of Fisch into the computer system of Kim and VESA in order to improve the efficiency of the hardware monitoring systems by systematically assigning a priority level to each of the multiple agents on a bus.

24. As to claim 18, the Graphics system for use in an Information Handling System (IHS) comprising all the limitations as discussed above in claim 8 characterized in that said graphics systems except that the combination of Kim and VESA fails to disclose an arbitration means having a first input connected to receive said first I^2C communication channel provided by said graphics engine, and having a second input for receiving a second I^2C communication channel provided by said hardware monitoring circuit; said arbitration means providing arbitration between said first and said second I^2C communication links so that the hardware monitoring circuit and the processor can both get access to said second receiving means of said at least one display. However, Fisch teaches the use of an initialization mechanism for symmetric arbitration agents (see arbitration unit 320 in Fig. 3). The arbitration counter of each bus agent is used to keep track of which agent was the last or current owner of the bus and which agent will be the next owner of the bus (col. 2, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the arbitration means of Fisch into the computer system of Kim and VESA in order to improve the efficiency of the hardware monitoring systems by systematically assigning a priority level to each of the multiple agents on a bus.

25. As to claim 19, the Graphics system for use in an Information Handling System (IHS) comprising all the limitations as discussed above in claim 9 characterized in that said graphics systems except that the combination of Kim and VESA fails to disclose an arbitration means having a first input connected to receive said first I^2C communication channel provided by said graphics engine, and having a second input for receiving a second I^2C communication channel provided by said hardware monitoring circuit; said arbitration means providing arbitration between said first and said second I^2C communication links so that the hardware monitoring circuit and the processor can both get access to said second receiving means of said at least one display. However, Fisch teaches the use of an initialization mechanism for symmetric arbitration agents (see arbitration unit 320 in Fig. 3). The arbitration counter of each bus agent is used to keep track of which agent was the last or current owner of the bus and which agent will be the next owner of the bus (col. 2, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the arbitration means of Fisch into the computer system of Kim and VESA in order to improve the efficiency of the hardware monitoring systems by systematically assigning a priority level to each of the multiple agents on a bus.

26. As to claim 20, the Graphics system for use in an Information Handling System (IHS) comprising all the limitations as discussed above in claim 10 characterized in that said graphics systems except that the combination of Kim and VESA fails to disclose an arbitration means having a first input connected to receive said first I^2C communication channel provided by said graphics engine, and having a second input for receiving a second I^2C communication channel provided by said hardware monitoring circuit; said arbitration means providing arbitration

between said first and said second I^2C communication links so that the hardware monitoring circuit and the processor can both get access to said second receiving means of said at least one display. However, Fisch teaches the use of an initialization mechanism for symmetric arbitration agents (see arbitration unit 320 in Fig. 3). The arbitration counter of each bus agent is used to keep track of which agent was the last or current owner of the bus and which agent will be the next owner of the bus (col. 2, lines 35-40). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the arbitration means of Fisch into the computer system of Kim and VESA in order to improve the efficiency of the hardware monitoring systems by systematically assigning a priority level to each of the multiple agents on a bus.

27. Claim 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim in view of VESA in further view of Fisch and in further view of Nelson U.S. Patent No. 5,768,612.

28. As for claim 11, Kim and Fisch do not specifically disclose an information Handling System according to claim 10 characterized in that said graphics systems is an ACP or PCI graphics card which is plugged into a corresponding AGP or PCI graphics slot having at least two wires which are dedicated for the communication of said second I^2C protocol communication channel. However, VESA discloses the I^2C communication link (page 1, Summary). Further more, Nelson discloses a graphic accelerator is a PCI graphics card which is plugged into a corresponding PCI slot having at least two conductors (col. 4 lines 14-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the I^2C communication link of VESA with the combination of Kim and Fisch in order to make it simple and easy to gather information about a computer's components. In addition, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the PCI buses of Nelson with the I^2C communication link of VESA, Kim and Fisch in order to utilized the high bandwidth and flexibility that is independent of new processor technologies and increases processor speed.

29. As for claim 12, information Handling System according to claim 11 characterized in that said graphics system and said processor are located on the same motherboard, which Nelson discloses the graphics accelerator and CPU are on the same motherboard (see figure 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thomas Pham; whose telephone number is (703) 305-7587 and fax number is (703) 746-8874. The examiner can normally be reached on Monday-Thursday and every other Friday from 7:30AM- 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Anil Khatri*, can be reached on *(703) 305-0282 or via e-mail addressed to [anil.khatri@uspto.gov]*. Any response to this office action should be mailed to: **Director of Patents and Trademarks Washington, D.C. 20231**, or **Hand-delivered** responses should be brought to **Crystal Park II, 2121 Crystal Drive Arlington, Virginia, (Receptionist located on the 4th floor),** or **faxed.** The following **fax numbers** apply:

Official	**(703) 746 - 7239**
Non Official/ Draft	**(703) 746 - 7240**
After Final	**(703) 746 - 7238**

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**thomas.pham@uspto.gov**].

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Thomas K. Pham
Patent Examiner

PAUL P. GORDON
PRIMARY EXAMINER

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June 27, 2003